Confirmation No. 5709

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	MATTHEWS, *et al.*	Examiner:	Daley, C.
Serial No.:	10/814,426	Group Art Unit:	2111
Filed:	March 31, 2004	Docket No.:	81339624US01
Title:	COMMUNICATION APPARATUS IMPLEMENTING TIME DOMAIN ISOLATION WITH RESTRICTED BUS ACCESS		

APPELLANT'S REPLY TO THE EXAMINER'S ANSWER

UNDER 37 CFR § 41.37

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

25235

Dear Sir:

This Reply to the Examiner's Answer is submitted pursuant to 37 C.F.R. §41.37, in support of the Appeal filed June 30, 2008.

No fees are believed due for filing this brief in support of the appeal as set forth in 37 C.F.R. §1.17(c). However, if necessary, authority is given to charge/credit Deposit Account 50-1123 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 018021/0819 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-56 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

All amendments have been entered.

V. Summary of Claimed Subject Matter

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a communication apparatus (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-7) comprising: a radio frequency (RF) circuit (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF circuit, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27); one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters; wherein access requests issued

by the one or more other bus masters to access the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF circuit (*see, e.g.*, page 12:16-22).

Commensurate with independent claim 21, an example embodiment of the present invention is directed to a method of operating a communication apparatus (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-7) including a radio frequency (RF) circuit (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7), the method comprising: arbitrating between requests to access a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27) by a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) and one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:24); receiving a signal indicative of a change in a mode of operation of the RF circuit (*see, e.g.*, page 12:16-22); and restricting access requests issued by the one or more other bus masters to access the bus in response to the signal (*see, e.g.*, page 12:16-22).

Commensurate with independent claim 26, an example embodiment of the present invention is directed to a mobile phone (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-25) comprising: a radio frequency (RF) transceiver (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF transceiver, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27); one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters; wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF transceiver (*see, e.g.*, page 12:16-22).

Commensurate with independent claim 32, an example embodiment of the present invention is directed to a mobile phone (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-25) comprising: a radio frequency (RF) front-end circuit (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF front-end circuit, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27) and one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters; wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF front-end circuit (*see, e.g.*, page 12:16-22); and wherein the RF front-end circuit and the digital processing circuit are fabricated on a single integrated circuit chip (*see, e.g.*, integrated circuit die 140 shown in Fig. 1, and page 6:26-27).

Commensurate with independent claim 38, an example embodiment of the present invention is directed to a communication apparatus (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-7) comprising: a radio frequency (RF) circuit (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF circuit, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27); one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters; wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a

signal asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit (*see, e.g.*, page 12:16-22).

Commensurate with independent claim 42, an example embodiment of the present invention is directed to a communication apparatus (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-7) comprising: a radio frequency (RF) circuit (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF circuit, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27); one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters according to an arbitration policy during at least a portion of a duration of an inactive mode of operation of the RF circuit; wherein the bus arbiter is further configured to implement a less favorable arbitration policy for the one or more other bus masters in response to a signal indicating a change to an active mode of operation of the RF circuit (*see, e.g.*, page 12:16-22 and page 19:12-23).

Commensurate with independent claim 49, an example embodiment of the present invention is directed to a mobile phone (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-25) comprising: a radio frequency (RF) transceiver (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF transceiver, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27); one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to allow accesses to the bus by the first bus master and the one or more other bus masters according to an arbitration policy implemented

during a first period of operation; wherein access requests issued by the one or more other bus masters to access the bus are restricted during a second period of operation in response to a signal asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit (*see, e.g.*, page 12:16-22).

Commensurate with independent claim 53, an example embodiment of the present invention is directed to a communication apparatus (*see, e.g.*, communication apparatus 100 shown in Fig. 1, and page 5:2-7) comprising: a radio frequency (RF) circuit (*see, e.g.*, RF front end circuit 110 shown in Fig. 1, and page 5:2-7) for operating on a radio frequency signal; and a digital processing circuit (*see, e.g.*, digital processing circuit 120 shown in Fig. 1, and page 5:2-7) coupled to the RF circuit, wherein the digital processing circuit includes: a first bus master (*see, e.g.*, MCU 302 shown in Fig. 3, and page 9:26-27) coupled to a bus (*see, e.g.*, AHB bus 310 shown in Fig. 3, and page 9:26-27); one or more other bus masters (*see, e.g.*, additional bus masters 312 shown in Fig. 3, and page 9:27 to page 10:6) coupled to the bus; and a bus arbiter (*see, e.g.*, arbiter 315 shown in Fig. 3, and page 10:1 6-24) configured to allow accesses to the bus by the first bus master and the one or more other bus masters according to an arbitration policy implemented during a first period of operation; wherein access requests issued by the one or more other bus masters to access the bus are restricted during a second period of operation beginning a predetermined amount of time prior to an active mode of the RF circuit (*see, e.g.*, page 12:16-22).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection to be Reviewed Upon Appeal

The remaining ground of rejection is listed below.

A. Claims 1-56 stand rejected under 35 U.S.C. § 103(a) over Shaeffer (U.S. Patent No. 6,963,626) in view of Hadwiger (U.S. Patent No. 6,738,845).

VII. Argument

Appellant maintains the request that the Board reverse the rejections of all pending claims because the cited combination does not correspond to the claimed invention and because the Examiner fails to provide sufficient detail regarding the proposed combination of the Shaeffer and Hadwiger references to enable Appellant to determine the propriety of the asserted combination.

The Examiner's interpretation of the claims in making the rejection of claims 1-56 under U.S.C. § 103(a) over Shaeffer and Hadwiger is both unreasonable and inconsistent with the specification and should, therefore, be reversed.

Section 2111 of the MPEP directs an examiner to interpret the claims of an application in its broadest reasonable interpretation consistent with the specification as would be interpreted by one skilled in the art. Specifically the MPEP states, "The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364[, 70 USPQ2d 1827] (Fed. Cir. 2004). Indeed, the rules of the PTO require that application claims must "conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description." 37 CFR 1.75(d)(1)."

The Examiner argues that paragraph 41 in combination with Figure 4B provides "the definition of restricting access [of] requests." Examiner's answer page 12. This is clearly not the case. Paragraph 41 in its entirety states:

> Thus, as illustrated in FIG. 4B, in one embodiment, to restrict access to AHB bus 310 by other masters 312, a restrict bus access signal is asserted a predetermined amount of time prior to a change to the radio active mode when (or shortly before) MCU 302 processes the interrupts. In response to assertion of the restrict bus access signal, arbiter 315 may cause any burst

transfers being performed by other bus masters 312 to be terminated early. In addition, further requests to access AHB bus 312 by masters other than MCU 302 may not be granted by arbiter 315, thus leaving MCU 302 with exclusive access to AHB bus 310 and the associated slave resources while the restrict bus access signal is asserted.

Claim 1 and the other independent claims of the present invention state in varying language, among other things, that "access requests issued … are restricted …." The embodiment claimed by the Appellant reflects an embodiment in which the arbiter restricts access requests issued by the one or more other bus masters. This interpretation is both reasonable and consistent with paragraph 41. The Examiner would have the Board believe that the claim should be interpreted to mean that the access requests are not restricted since the specification states in paragraph 41 that the arbiter "**may cause** other bus master activity to be terminated." Examiner's answer, page 12 (emphasis in original). The Examiner argues, "**This does not preclude the processor being fully terminated to meet the stated limitation**." Id. (emphasis in original)

The Appellant points out that it is that which is stated in the claims, interpreted in light of the specification, that the Appellant claims as his invention. The stated invention, with its imposed limitations, is consistent with the specification. The claims do not seek to broaden the role of the arbiter but to claim a specific embodiment of its function. That is, the arbiter's ability to restrict access to issued requests. Paragraph 41 clearly states that the arbiter possesses this ability. The Examiner attempts to broaden clearly stated limitations in the claims in order to fabricate a rejection based on Shaeffer and Hadwiger. This is clearly impermissible according to the MPEP and further, this type of claim construction has been addressed and dismissed as improper by the Federal Circuit.

The Federal Circuit in In re Zeltz, 893 F.2d 319 (Fed. Cir. 1989) held that it is incorrect to read an unwritten limitation into a claim. The Court stated, "During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow. When the applicant states the meaning that the claim terms are intended to have, the claims are examined with that meaning, in order to achieve a complete exploration of the applicant's invention and its relation to the prior art." See In re Prater, 415 F.2d 1393, 1404-

05, 56 CCPA 1381, 162 USPQ 541, 550-51 (1969) (before the application is granted, there is no reason to read into the claim the limitations of the specification). The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed. Burlington Industries, Inc. v. Quigg, 822 F.2d 1581, 1583, 3 USPQ2d 1436, 1438 (Fed.Cir.1987); In re Yamamoto, 740 F.2d 1569, 1571, 222 USPQ 934, 936 (Fed.Cir.1984). In re Zeltz at 322.

The Examiner's argument is without merit. A claim is to be given its broadest reasonable interpretation consistent with the specification. In this case the Appellant claims a function of an arbiter that is both reasonable and consistent with what is described in the specification. The Appellant seeks nothing more than that which is claimed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-56 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

Please direct all correspondence to:

CUSTOMER NO. **25235**

Respectfully Submitted,

By: _____

Name: Michael C. Martensen, Reg. No. 46,901

APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/814,426)

1. A communication apparatus comprising:
a radio frequency (RF) circuit for operating on a radio frequency signal; and
a digital processing circuit coupled to the RF circuit, wherein the digital processing circuit includes:
a first bus master coupled to a bus;
one or more other bus masters coupled to the bus; and
a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters;
wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF circuit.

2. The communication apparatus as recited in Claim 1 wherein the signal is indicative of a change to an active mode of operation of the RF circuit.

3. The communication apparatus as recited in Claim 2 wherein the signal indicates a change to a transmission mode of operation of the RF circuit.

4. The communication apparatus as recited in Claim 2 wherein the signal indicates a change to a reception mode of operation of the RF circuit.

5. The communication apparatus as recited in Claim 2 wherein the signal is asserted a predetermined amount of time prior to the change to the active mode of operation of the RF circuit.

6. The communication apparatus as recited in Claim 1 wherein the signal is asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit.

7. The communication apparatus as recited in Claim 1 wherein the signal indicative of a change of mode of operation of the RF circuit is generated by a timing circuit.

8. The communication apparatus as recited in Claim 1 wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal.

9. The communication apparatus as recited in Claim 1 wherein the first bus master is a microcontroller unit (MCU).

10. The communication apparatus as recited in Claim 1 wherein the first bus master is a digital signal processor (DSP).

11. The communication apparatus as recited in Claim 9 wherein an interrupt signal is provided to the MCU and wherein an interrupt service routine executed by the MCU in response to assertion of the interrupt signal is performed when accesses by masters other than the first bus master to the bus are restricted.

12. The communication apparatus as recited in Claim 11 wherein the interrupt service routine performs functionality to prepare the digital processing circuit for a shutdown mode of the digital processing circuit.

13. The communication apparatus as recited in Claim 1 wherein the bus is a multi-layer bus, wherein the first bus master is provided exclusive access to one layer of the bus in response to assertion of the signal while the one or more other bus masters are allowed access to another layer of the multi-layer bus.

14. The communication apparatus as recited in Claim 6 wherein the shutdown mode of operation includes disabling at least a portion of the digital processing circuit.

15. The communication apparatus as recited in Claim 6 wherein the shutdown mode of operation includes disabling a clock that clocks at least a portion of the digital processing circuit.

16. The communication apparatus as recited in Claim 1 wherein the bus arbiter is configured to restrict the granting of ownership of the bus to the one or more other bus masters in response to the signal.

17. The communication apparatus as recited in Claim 1 wherein the one or more other bus masters are configured to inhibit requests to gain ownership of the bus in response to the signal.

18. The communication apparatus as recited in Claim 1 wherein accesses by the one or more other bus masters are restricted by implementing a less favorable arbitration policy for the one or more other bus masters in response to the signal.

19. The communication apparatus as recited in Claim 1 wherein accesses by the one or more other bus masters to the bus are restricted by terminating burst transfers early in response to the signal.

20. The communication apparatus as recited in Claim 1 wherein the signal indicative of a change of mode of operation of the RF circuit is generated in response to execution of a software instruction.

21. A method of operating a communication apparatus including a radio frequency (RF) circuit and a digital processing circuit, the method comprising:

arbitrating between requests to access a bus by a first bus master and one or more other bus masters;

receiving a signal indicative of a change in a mode of operation of the RF circuit; and

restricting access requests issued by the one or more other bus masters to access the bus in response to the signal.

22. The method as recited in Claim 21 wherein accesses by the one or more bus masters are restricted by implementing a less favorable arbitration policy for the one or more bus masters in response to the signal.

23. The method as recited in Claim 21 wherein the signal is indicative of a change to an active mode of operation of the RF circuit.

24. The method as recited in Claim 23 wherein the signal is asserted a predetermined amount of time prior to the change to the active mode of operation of the RF circuit.

25. The method as recited in Claim 25 wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal.

26. A mobile phone comprising:

a radio frequency (RF) transceiver for operating on a radio frequency signal; and

a digital processing circuit coupled to the RF transceiver, wherein the digital processing circuit includes:

a first bus master coupled to a bus;

one or more other bus masters coupled to the bus; and

a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters;

wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF transceiver.

27. The mobile phone as recited in Claim 26 wherein the signal is indicative of a change to an active mode of operation of the RF transceiver.

28. The mobile phone as recited in Claim 27 wherein the signal is asserted a predetermined amount of time prior to the change to the active mode of operation of the RF transceiver.

29. The mobile phone as recited in Claim 26 wherein the signal is asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit.

30. The mobile phone as recited in Claim 26 wherein the signal indicative of a change of mode of operation of the RF transceiver is generated by a timing circuit.

31. The mobile phone as recited in Claim 26 wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal.

32. A mobile phone comprising:

a radio frequency (RF) front-end circuit for operating on a radio frequency signal;

a digital processing circuit coupled to the RF front-end circuit, wherein the digital processing circuit includes a first bus master coupled to a bus and one or more other bus masters coupled to the bus; and

a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters;

wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF front-end circuit; and

wherein the RF front-end circuit and the digital processing circuit are fabricated on a single integrated circuit chip.

33. The mobile phone as recited in Claim 32 wherein the signal is indicative of a change to an active mode of operation of the RF front-end circuit.

34. The mobile phone as recited in Claim 33 wherein the signal is asserted a predetermined amount of time prior to the change to the active mode of operation of the RF front-end circuit.

35. The mobile phone as recited in Claim 32 wherein the signal is asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit.

36. The mobile phone as recited in Claim 32 wherein the signal indicative of a change of mode of operation of the RF front-end circuit is generated by a timing circuit.

37. The mobile phone as recited in Claim 32 wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal.

38. A communication apparatus comprising:
a radio frequency (RF) circuit for operating on a radio frequency signal; and
a digital processing circuit coupled to the RF circuit, wherein the digital processing circuit includes:
a first bus master coupled to a bus;
one or more other bus masters coupled to the bus; and
a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters;
wherein access requests issued by the one or more other bus masters to access the bus are restricted in response to a signal asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit.

39. The communication apparatus as recited in Claim 38 wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal.

40. The communication apparatus as recited in Claim 38 wherein the shutdown mode of operation includes disabling at least a portion of the digital processing circuit.

41. The communication apparatus as recited in Claim 38 wherein the shutdown mode of operation includes disabling a clock that clocks at least a portion of the digital processing circuit.

42. A communication apparatus comprising:
a radio frequency (RF) circuit for operating on a radio frequency signal; and
a digital processing circuit coupled to the RF circuit, wherein the digital processing circuit includes:
a first bus master coupled to a bus;
one or more other bus masters coupled to the bus; and
a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters according to an arbitration policy during at least a portion of a duration of an inactive mode of operation of the RF circuit;
wherein the bus arbiter is further configured to implement a less favorable arbitration policy for the one or more other bus masters in response to a signal indicating a change to an active mode of operation of the RF circuit.

43. The communication apparatus as recited in Claim 42 wherein the signal is asserted a predetermined amount of time prior to the change to the active mode of operation of the RF circuit.

44. The communication apparatus as recited in Claim 42 wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal.

45. The communication apparatus as recited in Claim 42 wherein the first bus master is a microcontroller unit (MCU).

46. The communication apparatus as recited in Claim 45 wherein an interrupt service routine executed by the MCU in response to assertion of an interrupt signal is performed when the bus arbiter implements the less favorable arbitration policy for the one or more other bus masters

47. The communication apparatus as recited in Claim 46 wherein the interrupt service routine performs functionality to prepare the digital processing circuit for a shutdown mode of the digital processing circuit.

48. The communication apparatus as recited in Claim 42 wherein the RF circuit and the digital processing circuit are integrated on a single chip.

49. A mobile phone comprising:

a radio frequency (RF) transceiver for operating on a radio frequency signal; and

a digital processing circuit coupled to the RF transceiver, wherein the digital processing circuit includes:

a first bus master coupled to a bus;

one or more other bus masters coupled to the bus; and

a bus arbiter configured to allow accesses to the bus by the first bus master and the one or more other bus masters according to an arbitration policy implemented during a first period of operation;

wherein access requests issued by the one or more other bus masters to access the bus are restricted during a second period of operation in response to a signal asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit.

50. The mobile phone as recited in Claim 49 wherein the first bus master is provided exclusive access to the bus during the second period of operation.

51. The mobile phone as recited in Claim 49 wherein the shutdown mode includes disabling at least a portion of the digital processing circuit.

52. The mobile phone as recited in Claim 49 wherein the shutdown mode includes disabling a clock that clocks at least a portion of the digital processing circuit.

53. A communication apparatus comprising:
a radio frequency (RF) circuit for operating on a radio frequency signal; and
a digital processing circuit coupled to the RF circuit, wherein the digital processing circuit includes:
a first bus master coupled to a bus;
one or more other bus masters coupled to the bus; and
a bus arbiter configured to allow accesses to the bus by the first bus master and the one or more other bus masters according to an arbitration policy implemented during a first period of operation;
wherein access requests issued by the one or more other bus masters to access the bus are restricted during a second period of operation beginning a predetermined amount of time prior to an active mode of the RF circuit.

54. The communication apparatus as recited in Claim 53 wherein the first bus master is provided exclusive access to the bus during the second period of operation.

55. The communication apparatus as recited in Claim 53 wherein the second period of operation is controlled by a timing circuit.

56. The communication apparatus as recited in Claim 53 wherein the bus arbiter is configured to implement a less favorable arbitration policy for the one or more other bus masters during the second period of operation.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.